COMPACTING CIRCUIT RESPONSES

Abstract of the Disclosure

A compactor has a reduced number of outputs and the ability to handle a higher number of errors and unknown logic values. The procedure for designing the matrix and the resulting compactor involves determining the number of unknown logic values that may be encountered and adding columns to the compactor matrix based on the number of errors. Basically, the number of possible combinations of scan in lines is determined. Then, additional columns are added for each possible combination of scan in lines. The number of columns that are added for each combination of scan in lines is equal to the number of errors plus one in one embodiment.